## ABSTRACT OF THE DISCLOSURE

An apparatus and method provide for performing SIMD instructions (*i.e.*, multiply accumulate operations) using one MAC unit while minimizing the operational latency. In particular, the apparatus and method are accomplished by a MAC unit generating a first half of a data result and a second half of a data result. A deferred register stores the generated first half of the data result. A MISC unit is used to determine when to release the first half of a data result stored in the deferred register in order to synchronize the first half of the data result with the second half of the said result.